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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,200	09/16/2003	Uta Gebauer	MAS-FIN-115 D	1392

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,200	GEBAUER ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/047,028.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030916*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 6, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nelson** (4,930,216) in view of Beene et al. (5,673,478; hereinafter, "**Beene**").

Regarding claims 1, 6, 9 and 11:

Nelson discloses a method of fabricating an electronic component having semiconductor chips stacked on one another (e.g., note in Col. 4, lines 3-8, the inventions is also applicable to 3-D arrays) and connected via rewiring planes and through contacts formed at sawn edges of the semiconductor chip, the method comprising:

providing a semiconductor wafer with semiconductor chips (12a, 12b, 12c, 12d) arranged in rows and columns and sawing track regions 14 therebetween (note Figs. 1 and 5);

applying an insulating layer 32 for protection and for insulation of an active top side of the semiconductor chips (Fig. 6 and Col. 3, lines 17-21);

forming through contact holes (30a-3f) in the sawing track regions (Fig. 5), the through contact holes having a diameter greater than a width of a saw blade for dicing the semiconductor wafer (note the width of saw lines "38" and "40" in Fig. 9);

coating the inner wall of the through contact holes with at least one of an adhesion promoter and a solderable surface coating 34 by electroplating (copper or gold, note Col. 3, lines 30-35);

filling the through contact holes with an electrically conductive material (36a-36f) to form through contacts (Col. 3, lines 36-50);

patterning the insulating layer 32 (Fig. 7) by uncovering contact areas (22a, 22b) on the active top side of the chip and applying interconnects (36a-36f) for rewiring on the insulating layer 32, the interconnects (36a-36f) connecting individual contact areas to the through contacts (Figs. 8-9);

dicing the semiconductor wafer to form chips (12a-12d); and

in a case of forming a 3-D array, a plurality of chips (12a-12d) would be stacked to form an electronic component.

Nelson **lacks** specifically utilizing solder material for filling the through contact holes. Beene **teaches** a method of forming a 3-D electronic component utilizing solder material for connecting a plurality of chips that are stacked one on top of another. Beene teaches (in Col. 3,

lines 34-43) that solder is just one of a plurality of materials suitable for electrically connecting one chip to another within a stacked 3-D array/component. It would have been obvious to one of ordinary skill in the art to modify Nelson by specifically utilizing solder because Beene teaches that solder is just one of a plurality of materials suitable for connecting chips within a 3-D component; furthermore, it is noted that it has been held to be within the general skill of a worker in the art to select a known material (such as solder) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. *Specifically regarding claim 11:* Nelson discloses (in Fig. 11) forming solder deposits 45 in a case where the chip being bonded would serve as a bottommost chip.

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nelson** (in view of **Beene**) as applied to claim 1 above, and further in view of Haraichi et al. (5,055,696; hereinafter, "**Haraichi**").

Regarding claims 2 and 3:

Nelson (in view of Beene) **lacks** specifically forming the through contact holes by utilizing either reactive ion-beam etching or laser-beam etching; however, it is noted that Nelson specifies that the through contact holes may be formed using any suitable means (note Col. 3, lines 2-3). Haraichi is **cited primarily to show** that it was very well known in the art that either reactive ion-beam etching or laser-beam etching is suitable for forming contact holes. Haraichi discloses using both ion-beam etching and laser-beam etching for forming contact holes (note Figs. 30a-30b and Col. 22, lines 58-63). It would have been obvious to one of ordinary skill in the art to modify Nelson (in view of Beene) by specifically utilizing either ion-beam etching or

laser-beam etching because Nelson specifies that any suitable method may be used to form the through contact holes and Haraichi shows that it was very well known in the art that either ion-beam etching or laser-beam etching is suitable for forming contact holes.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nelson** (in view of **Beene**) as applied to claim 1 above, and further in view of **Bassous** (3,921,916).

Regarding claim 4:

Nelson (in view of Beene) **lacks** specifically forming the through contact holes by utilizing electrolytic cannula etching; however, it is noted that Nelson specifies that the through contact holes may be formed using any suitable means (note Col. 3, lines 2-3). Bassous is **cited primarily to show** that it was very well known in the art that electrolytic etching is suitable for forming holes in a semiconductor substrate (note Col. 5, lines 48-53). It would have been obvious to one of ordinary skill in the art to modify Nelson (in view of Beene) by specifically utilizing electrolytic etching because Nelson specifies that any suitable method may be used to form the through contact holes and Bassous shows that it was very well known in the art that electrolytic etching is suitable for forming holes in a semiconductor substrate.

6. Claims 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nelson** (in view of **Beene**) as applied to claim 1 above, and further in view of Givens et al. (6,080,655; hereinafter, "**Givens**").

Regarding claims 5, 7 and 8:

Nelson (in view of Beene) **lacks** coating the inner walls with titanium or titanium alloy and coating the inner walls with a vapor deposition process (CVD or PVD). Givens **teaches** coating the inner walls of a contact hole by using titanium provides good bonding (note Col. 5, line 65 to Col. 6, line 3). Givens also discloses (in Col. 5, lines 34-48) that a conductive layer may be deposited within a contact hole by using CVD, PVD, or electrochemical processes, i.e., these processes are very well known in the art and it would be an obvious matter of design choice to utilize any of one of them (note that Nelson specifies using an electrochemical process for coating the inner walls). It would have been obvious to one of ordinary skill in the art to modify Nelson (in view of Beene) by using titanium or a vapor deposition process because titanium would provide a good bond (as taught by Givens) and it would be an obvious matter of design choice to use vapor deposition instead of the electrochemical process specified by Nelson, since Givens shows that either vapor deposition or an electrochemical process is suitable for depositing a conductive material into a contact hole.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Nelson** (in view of **Beene**) as applied to claim 1 above, and further in view of Inoue et al. (5,270,493; hereinafter, "**Inoue**").

Regarding claims 2 and 3:

Nelson (in view of Beene) **lacks** screen printing the interconnects; however, note that Beene discloses conductive materials such as conductive epoxy can be used for the interconnects (Col. 3, lines34-38). Inoue is **cited primarily to show** that material such as conductive epoxy is

widely available and when utilized, such materials would be screen printed (note Col. 8, lines64-68). Nelson in view of Beene discloses the general conditions of the instant claim; therefore, it would have been obvious to one of ordinary skill in the art to modify Nelson (in view of Beene) by specifically reciting that the intereconnects are screen printed because Inoue shows that at least one of the materials specified by Beene would be applied by screen printing.

Allowable Subject Matter

8. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Claims 12 and 13 would be allowable primarily because claim 12 requires a plurality of semiconductor wafers to be connected as recited in claim 1, and subsequently separating the stacked wafers to form stacks of chips.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 are cited to show methods of forming a stacked electronic component with process steps similar to those of the current invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Thu (1 PM - 9:30PM EST) and Sat.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

July 9, 2004

MATTHEW SMITH
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